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Current perspectives

Device implications of spin-transfer torques

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Abstract

This article examines spin-transfer torques from the perspective of three technological applications: hard disk drives, magnetic random access memory (MRAM), and current-tunable high-frequency oscillators. In hard disk drives, spin-transfer torques are a source of noise, and we discuss the implications spin-transfer noise will have on future sensor designs. For MRAM, we evaluate the feasibility of spin-transfer-driven switching. Finally, we discuss the possibility of GHz communication applications enabled by nanoscale spin-transfer oscillators.

keywords: GMR; TMR; MRAM; Magnetic recording; Spin transfer; Oscillators

1. Introduction

As a result of theoretical predictions [1,2] and early experimental verification [3,4] of spin-transfer torques, there has been tremendous excitement about its potential for device applications. Such excitement is natural—magnetism is widely used in commercial devices, and the spin-transfer effect provides a local means of manipulating magnetization rather than relying on the long-range effects mediated by a remote current via its Oersted field. As the other articles in this issue demonstrate, remarkable progress has been made in the area of spin-torque research over the past decade. However, spin-torque-based devices have not been introduced in the market as yet. This is not surprising. Even in the most favorable conditions, it often takes more than 10 years to commercialize new phenomena. The giant magnetoresistance (GMR) read head was first introduced in 1997 some 11 years after initial reports of GMR in the literature [5,6]. Similarly, room temperature magnetic tunneling was demonstrated in 1995 [7] and only in the last 1 or 2 years have tunneling read heads and magnetic random access memory (MRAM) cells been commercially available. Based on these examples, the commercial impact of spin torque may be expected in the near future.

High-density MRAM and current tunable high-frequency oscillators are applications for which the spin-transfer effect could find commercial viability. In this article, we will offer our perspective on these two applications, including a discussion of the key technical challenges that must be overcome before these technologies can be commercialized. In addition we will describe the detrimental impact of spin torque on GMR devices, especially on applications which require small sizes and high current densities such as next generation GMR read heads.

The basic phenomena of spin torque occur for current flowing through two magnetic elements separated by a thin non-magnetic spacer layer. The current becomes spin polarized by transmission through or upon reflection from the first magnetic layer (the reference layer) and mostly maintains this polarization as it passes through the non-magnetic spacer and enters and interacts with the second ferromagnetic layer (the free layer). This interaction leads to a change of resistance depending on the relative orientation of the magnetic layers giving rise to GMR. Commensurate with the GMR, there is a transfer of angular momentum from the polarized current to the free layer magnetization that can be described as an effective torque.

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This spin torque can oppose the intrinsic damping of the magnetic layer exciting spin waves and, for sufficient current strengths, reverse the direction of the magnetization.

In general, spin torque and GMR are intimately linked. That is, it is difficult to have one without the other. From an applications point of view, this can have significant detrimental implications in GMR-based devices. For GMR magnetic sensors and read heads, the magnetic layers are designed such that one layer is rather insensitive to an external field (the reference layer) and the second layer responds to an external field (the free layer). Implicit in these designs is that the current only monitors the relative angle of the magnetization of the two layers (via the GMR effect and change in resistance) and only affects the magnetization via heating and the generation of Oersted fields. However, spin-torque effects couple the magnetization of the reference and free layers. As a result, the magnetic recording industry is all too familiar with spin-torque-induced excitations as a source of noise in magnetic recording head sensors. It is in these sensors where spin-torque effects are likely to have their first commercial impact, albeit negative, so we will begin by discussing the implication of spin torques on proposed GMR sensor technologies, before moving onto two applications, spin–transfer-driven MRAM and current-tunable oscillators, that are enabled by spin-torque effects.

2. Spin-torque effects in CPP-GMR sensors

Relative to applications such as MRAM, little has been published on spin-torque effects in hard disk drives. Interestingly, in addition to latches and oscillators, John Slonczewki's original (rather cryptically titled) spin-torque patent described using the spin-torque effect to write bits on the recording media in disk drives [8]. Although the spin-torque effect in theory could allow one to write bits with better resolution than can be achieved by the fields generated from the pole tip of a recording head, the challenge of making reliable electrical contact to a disk rotating at nearly 10,000 rpm beneath the head appears to make this impractical.

As mentioned in the introduction, it is spin-torque effects in the sensor that presently cause concern for the disk drive industry. As we write this paper, the hard disk drive industry is changing its sensor geometry, moving from the presently used current-in-plane (CIP) GMR sensor [9] to a current-perpendicular-to-the-plane (CPP) tunneling magnetoresistive (TMR) sensor [10]. In a CIP sensor the current flows within the film plane which is the easiest geometry to employ in a film or when the lateral size of the device is large compared to the thickness of the layers. In CPP devices, the current leads are at the top and bottom of the film stack and the current flows perpendicular to the layers. This geometry is only feasible for high resistance film stacks (e.g. magnetic tunnel junctions) or for low resistance (i.e. fully metallic) film stacks with confined lateral dimensions less than 100 nm. This transition is driven by a number of factors, which include the higher magneto-resistance ratios achievable in TMR junctions and the ease in lithographic definition. A CIP-GMR read head is shown in Fig. 1a and described in detail in Ref. [9]. The magnetic field sensitivity is derived from the GMR stack that consists of a reference layer that is relatively insensitive to external field and a free layer that responds to a field. The relative angle of the magnetization of the reference and free layers controls the resistance of the device.

In present read heads the reference layer is an antiparallel coupled Co/Ru/Co stack exchange biased by an antiferromagnetic layer. Such a reference layer structure is also used in MRAM technologies [11]. The coupling is mediated by a ~0.7 nm Ru layer whose thickness is tuned to couple the layers via an RKKY interaction [12]. The two Co layers are nearly the same thickness such that net moment of the Co/Ru/Co stack (the difference of the two layers magnetization) is small. This has two advantages. The low moment of the stack limits the dipole fields generated by the reference layer that interact with the free layer. Second, the low moment makes the reference layer react weakly to external fields as long as the fields are weaker than the antiparallel exchange coupling strength. The Co/Ru/Co net magnetization direction is maintained

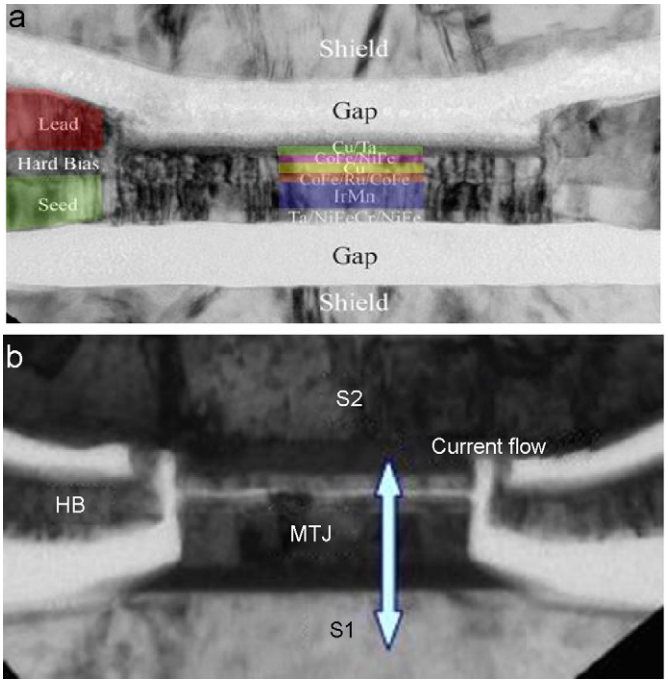

Fig. 1. (a) Transmission electron microscopy cross-section of a CIP read head sensor. False color has been added to help distinguish the various metallic layers from one another. Trackwidth is approximately 130 nm. (b) Transmission electron microscopy cross-section of a magnetic tunnel junction (MTJ) read head sensor. The bottom and top leads of the sensor are the magnetic shields *S*1 and *S*2. The sense current flows between these two leads. Alumina (bright in image) insulates the hard bias (HB) from the sensors and the shields. The tunnel barrier is the bright line approximately co-linear with the HB. The trackwidth is approximately 80 nm.

by coupling the device to an antiferromagnetic layer (e.g. IrMn or PtMn) [9]. The direction is set by annealing the device in a field. For a read head, the orientation of the reference layer is into/out of the plane of the picture. The free layer is a Co/NiFe (or CoFe/NiFe) composite layer separated from the reference layer by a Cu spacer. The composite is used to optimize both the transport and magnetic properties. Co layers give high GMR values when coupled with Cu, but do not have optimal magnetic properties (e.g. Co can be magnetically hard and sensitive to strain via magnetostriction). The combination of Co/NiFe maintains the GMR amplitude but is magnetically softer (responds more readily to low fields) than Co and is less sensitive to strain.

The GMR stack is lithographically patterned to form the sensor where the width is known as the physical track width because this dimension determines the read back resolution across the data tracks on the disk. This is the minimum lithographic feature in the read head. The equilibrium alignment of the free layer is perpendicular to the reference layer and is stabilized by the dipolar field provided by the hard bias layers deposited on either side of the sensor. This 90° orientation of the free and reference layers provides the highest sensitivity and makes the resistance roughly linear for small fields (i.e. small angular deviations from 90°). For CIP sensors the current leads are connected to the edge of the sensors and the current flows within the plane of the film. A thin (~10 nm) alumina layer is deposited on either side of the sensor which electrically insulates the sensor from the conductive magnetic shields. The spacing of the shields provides the down track spatial resolution.

As stated earlier, there is a transition underway from the CIP sensors to CPP sensors. This results from a number of factors, including the TMR response being significantly higher than that in CIP-GMR structures. In addition, the current leads are connected to the edge of a CIP device, which adversely affects the response of the sensor near the edge, giving rise to degradation of performance with decreasing sensor dimensions [13]. For TMR sensors (and CPP sensors, in general) the top and bottom shields also serve as the top and bottom electrical contacts to the sensor eliminating these edge effects. An example of a TMR read head sensor is shown in Fig. 1b. The sensor is electrically isolated on its sides from the hard bias layers confining the current to flow normal to the layers. The magnetic sensitivity arises from the tunneling conductance across the thin insulating layer. Similar to GMR, the TMR response depends on the relative angle of the magnetic layers on either side of the insulating layer that forms the magnetic tunnel junction (MTJ). In early 2007, state-of-the-art TMR sensors will have physical trackwidths of ~80 nm and support recording densities of approximately 130 Gbit/in^2.

While the CPP geometry has a number of advantages for high-density applications, in this geometry sensors become more susceptible to spin-torque effects. For state-of-the-art TMR sensors, spin-torque effects are not, as yet, a significant problem. The resistance of a TMR sensor is controlled by the resistance of the tunnel junction times the junction area (the RA product). This value is typically on the order of 3 Ω μm^2 and results in low current densities. Even for a TMR sensor with an extremely low RA-product of 1 Ω μm^2, when operated at a 120 mV bias, its current density is 1.2×10^7 A/cm^2, which is generally well below the threshold for inducing spin-torque excitations. Note that with track width and stripe height both equal to 80 nm, this 1 Ω μm^2 sensor has a resistance of around 150 Ω.

Consider, then, the target dimensions of a sensor for a disk drive with storage densities of 500 Gbit/in^2, which are projected to be around 30 nm per side. Even if the RA-product of the TMR sensor could be lowered to 1 Ω μm^2, the resistance would still exceed 1000 Ω, which, for impedance matching reasons, is impractical for high data rate applications. For a given materials set, the resistance of the tunnel junction scales exponentially with the barrier thickness. Lower RA values can be obtained by thinning the barrier. The minimum resistance is set by how thin a reliable barrier can be made that maintains tunneling. This is currently on the order of a few monolayers so continued thickness reductions will be challenging. In the absence of the discovery of reliable, ultralow RA tunnel barriers, there is an expected transition from CPP-TMR to metallic CPP-GMR sensors. A fully metallic CPP-GMR sensor might have an RA-product of ~0.05 Ω μm^2, corresponding to a sensor resistance between 50 and 100 Ω at 500 Gbit/in^2 dimensions. Unfortunately, fully metallic sensors will almost certainly never achieve the very large (~100% and higher) $\Delta R/R$ values presently available in MgO tunnel valves, so significantly higher current densities must be used to achieve sufficient signal-to-noise ratio in the sensor. In general, more current means more signal. In state-of-the-art metallic CIP-GMR heads the current densities are 3×10^8 A/cm^2. What will limit the currents used in CPP-GMR sensor?

While heating and electromigration are concerns at high current densities, the onset of spin-torque effects is viewed as a significant barrier to high currents. In Fig. 2, we show a schematic of a prototype CPP-GMR read head from several perspectives. Fig. 2a shows the view from the surface of the disk (the air baring surface) which corresponds to the transmission electron microscopy images in Fig. 1. Fig. 2a and b display cross-sectional cuts showing the magnetic layers. Note that the sensor stack bears an uncanny resemblance to devices that have previously been used to study spin-torque effects [14]. In fact, the only significant difference between the CPP-GMR sensor in Fig. 2 and the devices in Ref. [14] is the relative orientation between the free and reference magnetic layers. In the absence of field excitations from the media, hard magnets on either side of the sensor free layer align that layer orthogonal to the reference layer as in a CIP sensor. If we call the relative angle between the reference and free layers ϕ, the media excitations typically would excite

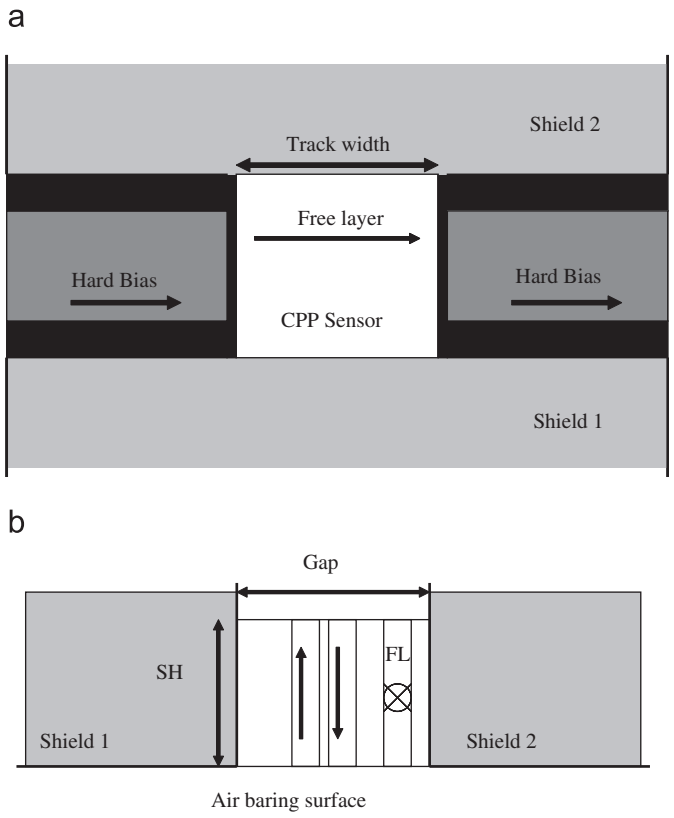

Fig. 2. Schematic representations of a CPP GMR read head sensor. (a) an air baring surface view of the sensor where the insulating layer between the hard bias and the sensor is drawn in black. (b) device cross-section highlighting the relative orientations of the free layer and antiparallel-pinned layers. (c) Generic CPP GMR sensor stack. The dark line separating the pinned and reference layers is the thin Ru coupling layer.

$\phi \pm 20^\circ$ about the equilibrium to provide a linear response of resistance with field [9].

Neil Smith et al. [15] analyzed the angular dependence of spin-torque CPP-GMR read heads to determine critical currents required to excite precession dynamics in the free layers resulting in a dramatic increase in the noise. In a simplified model that fairly accurately approximates the sensor, one can assume the reference layer magnetization is fixed and polarizes the current. The hard bias layers provide a uniform field, H_{ip}, in the plane of the free layer. The free layer is assumed to act as a uniformly magnetized single domain, with net out-of-plane uniaxial stiffness $H_\zeta(\sim 4\pi M_s - H_{k\zeta})$ where $4\pi M_s$ is the shape anisotropy of a thin film and $H_{k\zeta}$ and out-of-plane magnetic anisotropy of the free layer that counters the shape anisotropy. In this approximation, J_e, the critical current density for spin-torque-driven instabilities in the free layer is given by

$$J_e(q) \cong \frac{(M_s t)_{free}}{\hbar/2eP} \frac{(2|H_{ip}| + H_\perp)\alpha}{(1-q^2)d\beta/dq - 2q\beta(q)}, \quad (1)$$

where q is $\cos(\phi)$, α is the Gilbert damping coefficient, P is the spin polarization of the magnetic layers, and β is a numerical coefficient proposed by Slonczewski to describe the angular dependence of the spin-transfer torque [2]. In the MRAM devices discussed later in this paper, the switching is between parallel and anti-parallel magnetization (q near 1), so the derivative of β has negligible impact on the stability analysis. Conversely, in a CPP sensor the free layer is typically oriented so that q is between 0 and 0.5, and both β and its derivative have a strong effect on J_e, so finding the optimal bias angle and current polarity are important for minimizing spin-torque effects in the sensor. This is complicated by the fact that β depends on many details of the structure (e.g. layer thicknesses and materials, spin-diffusion lengths, etc.). Using reasonable values of $H_{ip} = 700\,\text{Oe}$, $H_\zeta = 8\,\text{kOe}$, $\alpha = 0.02$, and $P = 0.3$, J_e is predicted by Eq. (1) to be $\sim 1.2 \times 10^8\,\text{A/cm}^2$, although in practice temperature effects and non-uniform free layer magnetizations tend to lower this value [16]. Even $1.2 \times 10^8\,\text{A/cm}^2$ only corresponds to a 60 mV bias for a $0.05\,\Omega\,\mu\text{m}^2$ sensor, which will likely not provide enough signal for a $500\,\text{Gbit/in}^2$ sensor.

In this geometry, increasing the polarization of the magnetic layers will increase the GMR signal. There is significant research into half-metallic materials (i.e. 100% spin polarization) such as magnetic oxides and Heusler alloys that provide larger $\Delta R/R$ and more signal for a given bias voltage [17]. Unfortunately, the higher signal in such alloys results from higher polarizations, which results in a concomitant lowering of the threshold voltage for spin-torque excitations (Eq. (1)). Nevertheless, such high polarization materials may prove useful if other techniques could be employed to mitigate spin-torque effects.

One option being pursued to increase the bias voltage achievable in CPP-GMR sensors is exploring materials with higher RA products. Hypothetically, a material with otherwise identical properties (same α, P and $\Delta R/R$) but an RA product of $0.2\,\Omega\,\mu\text{m}^2$ would generate four times the signal at an acceptable $300\,\Omega$. Recently, there has been work published on CoFeAl alloys [18] that increase the RA-product while maintaining the spin polarization.

Another approach might be to increase the damping coefficient α. In principle, the GMR response of the sensor should be relatively insensitive to the damping parameter of the free layers (although the thermal magnetic noise would increase with higher damping [19]). However, J_e scales linearly with α. In thin permalloy films, light doping with Tb has been shown increase of α by over an order of magnitude [20]. In 2% Tb doped permalloy free layers, researchers at Cornell have recently demonstrated a factor of three increase in the low-temperature critical currents for

spin-transfer reversal of the free layer, without any loss of $\Delta R/R$ [21]. If a similar suppression of the critical currents could be achieved in CPP-GMR sensors, it could allow higher operating voltages and signals. Our experience with CIP sensors informs us that current densities of at least 2.5×10^8 A/cm^2 can be used before electromigration and heating effects would limit sensor operation. In addition, at 30 nm dimensions, self-fields (the field generated by the current in the sensor) are far less than H_{ip}, and therefore impose no current density limitations. For future sensor development, additional research is needed to understand how to control and optimize the polarization, damping, and resistance of materials while maintaining the relatively soft magnetic properties required of the free layer.

Yet another means of minimizing spin-torque excitations in the free layer is to modify the geometry of the head to minimize the impact of spin torque. One example is the dual-spin-valve geometry as shown in Fig. 3. This design has two reference layers, located symmetrically above and below the free layer. Assuming the reference layers are aligned with one another and the spin-dependent scattering is the same at both the top and bottom free layer interfaces, one expects the spin-transfer torques to cancel one another. Furthermore, the $\Delta R/R$ values of such sensors are typically 1.5 times that of simple spin valves (the added parasitic resistance of the top AFM layer limits some of the expected 2 times benefit). In practice, perfect spin-torque cancellation is not to be expected, however, researchers at Hitachi have shown that the cancellation appears complete enough so that it is the spin-torque excitations in the reference layers rather than the free layer that limit the bias voltage that may be applied to these dual sensors [16,22].

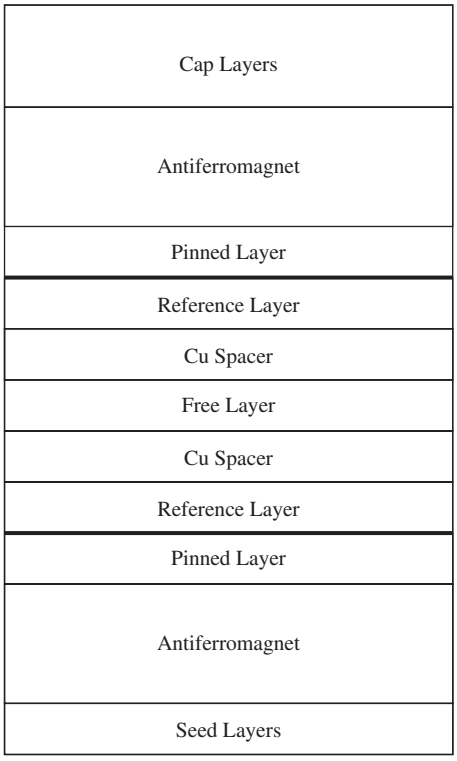

Fig. 3. Schematic representation of a generic CPP GMR dual sensor. The pinned layer magnetizations are set parallel to one another.

Before we celebrate the triumph of the dual-spin-valve, there are limitations to this design. In order to add the required additional layers to the stack the total thickness of the sensor is increased significantly. To accommodate the extra thickness of the sensor the shields need to be further apart. The recording head flies over the disk at a fixed height such that the separation between the shields (the so-called read gap) limits the ability of sensor to resolve individual bits along the direction of motion. Hence, increasing the read gap will degrade the resolution of the sensor and therefore lower the storage density capability of the system. For the structure in Ref. [22], the separation between the shields increased to 50 nm. However, system designs project a 35 nm separation will be required for a 500 Gbit/in^2 sensor. Therefore, considerable progress needs to be made before a dual-spin-valve can be squeezed into a 500 Gbit/in^2 read head. Simply reducing the thicknesses of the layers leads to thermal instability of the reference layers [23] and thermal magnetic noise in the free layers [19].

So what will the first 500 Gbit/in^2 sensor design be? At the moment this is still an open question. The challenge in this application is to generate a sufficient signal voltage ($\sim$1 mV) from a cube of material roughly 35 nm per side, thermally stable and operating at current densities low enough so that spin-torque-driven excitations do not degrade the signal-to-noise ratio.

3. Spin-transfer-driven MRAM

The potential application most often associated with spin transfer is ST-MRAM (spin-transfer MRAM). Two startup companies (Grandis and MagIC, both in Milpitas, CA) have been formed to pursue this application. In addition, large semiconductor companies such as IBM, Freescale, Sony, and Hitachi have efforts in this area. To understand the appeal of ST-MRAM, it is useful to look at the toggle MRAM technology that recently has been commercialized by Freescale [24]. In the earliest forms of MRAM the bit state is programmed to a "1" or "0" by aligning the magnetization of the free layer either anti-parallel or parallel to the top magnetic layer of the reference. This writing is achieved by passing a current down the 'bit line' (Fig. 4a) that generates a magnetic field that is aligned along the magnetic easy axis of the bit. However, as all the bits along a bit line are exposed to this field (known as half-selected bits), its magnitude is chosen to be below the threshold for writing. A second current pulse is sent down the 'write line' that is orthogonal to the bit line (known as a cross point architecture). Where the bit and write lines cross, there is sufficient field to write the bit. A limiting factor for this approach arises from distributions in magnetic materials. Due to process and material variations, patterned magnetic arrays have distributions of switching fields which tend to broaden as the size of the

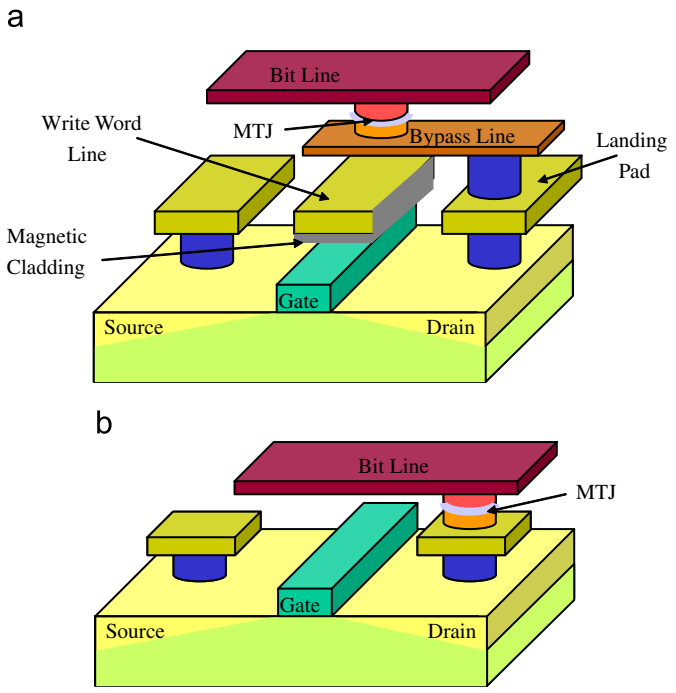

Fig. 4. Comparison of conventional toggle field-switched MRAM cell (a) and ST-MRAM cell (b) The ST-MRAM eliminates the need for a remote write line and a bypass line, allowing for a more compact architecture [56].

device shrinks. For successful programming the write field distributions need to be sufficiently narrow to allow the writing of a selected bit without disturbing the other half-selected bits. In addition, even if the field is not sufficient to write a half selected bit, the field lowers the energy barrier and makes the bit more susceptible to thermal activation during writing.

To address this half-select problem, Freescale introduced a toggle writing mode. In the toggle MRAM design, the free layer is a compensated antiferromagnetically coupled layer (e.g. Co/Ru/Co) similar to what is used in the pinned layers. However, the coupling between the two layers is tuned to be weaker than that used for the reference layer such that the magnetic layers cant in the applied fields from the bit and write lines (this canting is known as a spin flop for antiferromagnetic materials). The writing is achieved by a sequence of pulses that first sends current down the write line followed by the bit line. The current is then turned off first to the write line followed by the bit line. By following this procedure, the coupled free layer cants towards fields from the write and bit lines. For the bit at the cross point, the net magnetization follows the rotating net field and reverses the direction of the magnetization. The procedure does not write a given direction but simply changes the direction of the bit. Thus, the programming is achieved by first reading a bit and then reversing the bits in the incorrect state. The advantage of this approach is that the half selected bits simply cant in the field, but do not reverse their magnetization. This unique behavior results in a much wider operating window.

For readback, tunnel junctions, rather than metallic spin valves, are necessary in MRAM because their larger resistances and signal voltages allow high-speed read operation with CMOS circuitry. In addition the tunneling signal is only sensitive to the magnetization of the layer adjacent to the barrier allowing the magnetization of the compensated free layer to be determined. Because of the remote write lines, toggle MRAM cannot match the storage density of flash, which is the mainstream non-volatile semiconductor memory. But unlike flash, MRAM is fast (~20 ns write and read time) and has excellent write endurance ($>10^{15}$ cycles), so MRAM has the potential to replace battery-backed SRAM. In addition, MRAM is an attractive option for embedded, high-performance memory applications.

Unfortunately, toggle MRAM may not be expected to scale well to small dimensions. As the size of the bits shrink, the fields from the bit and write lines fall off inversely with the feature size assuming a constant current density. Therefore, it is expected that the currents required to write the bits must grow. The larger current requirements will limit the number of elements that can be arrayed and degrade the layout efficiency of the memory. In addition, the higher write currents will increase the power consumption well beyond that of SRAM or DRAM. ST-MRAM has the potential to ease many of the scaling limitations of current toggle MRAM, opening potential applications and markets.

As illustrated in Fig. 4b, ST-MRAM does not use an external write line; instead current is injected directly into the tunnel junction where the spin-transfer effect is used to write the bits. In spin–transfer-driven switching, it is the current density, not the current, that determines the threshold for writing a bit, so ST-MRAM does not have the scaling problems that limit toggle MRAM. In fact, the elimination of the separate write line should lower the power consumption below that of either SRAM or DRAM and allow a compact cell size that could, in principle, approach the storage density of flash [25]. In theory, then, ST-MRAM could be fast, dense, low-power, and non-volatile—the "universal" memory that IC designers dream of. The crucial question, of course, is what technological barriers stand in the way of realizing these applications?

For a memory to work, you must be able to reliably read and write the bits. Toggle MRAM has proven that MTJs can be reliably read without endurance issues. Reading is slightly more troublesome in ST-MRAM because the sense currents are now going to be driven through a junction designed to be switched via spin torque with as low a current density as possible. In addition, there needs to be a safe working margin so that the current density always sufficient to successfully read a bit is never able to write that same bit. Finally, the voltage needed to obtain spin-torque writing needs to be low enough not to damage or degrade the barrier. As discussed below, high-density ST-MRAM may someday be written at currents densities as low as 5×10^5 A/cm^2, so would say 1×10^5 A/cm^2 be an

acceptable read current density? Until recently, this may have posed a problem, but the development of MgO tunnel junctions with well over 100% $\Delta R/R$ for RA products as low as $2\,\Omega\,\mu m^2$ should allow high-speed read operation safely below the writing threshold.

Writing the bits may prove to be more problematic. The first observation of spin-transfer switching in spin-valve systems was at current densities well over $10^7\,A/cm^2$. These metal systems could withstand current densities $>2\times10^8$ A/cm^2 before endurance would be a concern, however, MgO tunnel barriers will start to have endurance problems around $1\times10^7\,A/cm^2$, so for ST-MRAM to be at all viable, it is necessary to have a switching current below this value. Fortunately, as we will describe below, recent work seems to indicate that achieving this threshold should be possible. In addition, as tunnel junctions are increasingly used in read heads, there will be new understanding of tunnel junction performance with high current densities.

In order to achieve the highest possible memory density, one would like the bit to switch with the current that can be provided by a single transistor whose channel width is equal to the width of the MTJ. Assuming the transistor can source 0.5 mA of current per micron of channel width, an MTJ with a 2×1 aspect ratio would need to switch at $5\times10^5\,A/cm^2$ in order to use a single, minimal width transistor. Is this feasible?

Eq. (2) is an expression for I_c, the critical current required to induce spin-transfer reversal at zero temperature in a macrospin approximation assuming a collinear geometry [26] with the magnetization of the layers in the film plane,

$$I_c = \left(\frac{2e}{\hbar}\right)\left(\frac{\alpha}{\eta}\right)M_s V(H + H_k + 2\pi M_s), \tag{2}$$

where H is the field applied along the easy axis (also the uniaxial anisotropy direction including the dipole field from the reference layer), M_s and V are the magnetization and volume of the free layer, respectively, and H_k is the anisotropy field. The spin-transfer efficiency, η, is a function of the current polarity, polarization, and the relative angle between the free and pinned layer. An interesting feature of spin-transfer-induced switching is that the switching speed depends on the duration and amplitude of the current pulse [27,28]. For room temperature operation, the I_c of Eq. (2) corresponds to switching times in the 5–20 ns range. Thermal excitations, however, will allow reversal at currents well below I_c. Such thermally assisted switching is relatively slow, but, depending on the application, one may be willing to trade write-speed for the higher storage density a lower I_c can allow. After all, program times for flash are typically at least 100 μs. Conversely, to achieve ultra-fast operation comparable to the 1 ns write times of SRAM, current pulses several times larger than I_c are required.

For typical free layer materials like CoFe, the sum of the three field-like terms in Eq. (2) is dominated by the shape anisotropy field $2\pi M_s$ (~8 kOe). This term does not contribute to the stability of the bit to thermal excitations which is proportional to H_k. One means of lowering I_c would be to use a freelayer incorporating additional perpendicular magnetic anisotropy ($H_{k\perp}$) that compensates the shape anisotropy. For $H_{k\perp}<4\pi M_s$ the stable configuration for the magnetization is still in the film plane, but the $2\pi M_s$ in Eq. (2) is replaced by $2\pi M_s$–$H_{k\perp}/2$ [29]. For $H_{k\perp}>4\pi M_s$ the magnetization is out of the film plane, which would eliminate the $2\pi M_s$ term in Eq. (2); in this case H_k becomes the effective perpendicular anisotropy $H_{k\perp}$–$4\pi M_s$. In metallic systems, efficient current driven reversal has been demonstrated in systems with out-of-plane anisotropy [30], so it is not implausible to believe similar films may be adapted to tunnel junctions. To substantially lower I_c, however, one needs to lower the anisotropies below those currently used to achieve the out of plane magnetization. While it is possible to tune the anisotropy of materials, the net anisotropy of a perpendicular film is the difference between two relatively large numbers ($H_{k\perp}$ and $4\pi M_s$). So a small H_k will require a careful balancing of these terms, and this may result in large bit-to-bit variations.

Assuming it is possible to substantially lower the shape anisotropy term in Eq. (2), thermal stability requirements for the sensor would still impose a lower bound on H_k. For 10 year thermal stability, the anisotropy energy, U_k must be around $60k_BT$. For a macrospin with uniaxial anisotropy, $U_k = M_s V H_k/2$, so, in the absence of the $2\pi M_s$ term, Eq. (2) reduces to

$$I_c \approx \left(\frac{2e}{\hbar}\right)\left(\frac{\alpha}{\eta}\right)U_k. \tag{3}$$

The coefficients α and η are obviously critical to determining I_c. During the fabrication process, there is evidence that surface oxides or other effects increase the damping coefficient substantially from its value in continuous thin films [31] and perpendicular films also often have higher α values. However, it is not unreasonable to believe a damping coefficient on the order of 0.01 is achievable. Recent measurements at Grandis show that the polarization in MgO MTJs is substantially higher than that found in Al_2O_3 junctions, and correspond to η around 0.25 [32]. Using $\alpha = 0.01$ and $\eta = 0.25$, $U_k = 60k_BT$ in Eq. (3) corresponds to I_c~30 μA, or J_c~$6\times10^5\,A/cm^2$ for a 50×100 nm MTJ. Note, though, that I_c does not depend on the sample area, so thermal stability constraints may limit the ultimate areal density one can achieve in ST-MRAM.

For effective bipolar operation, the film stack shown in Fig. 5a would be a poor choice, because the critical currents would be approximately 50% higher when electrons flow from the free layer to the pinned layer than they would be when the polarity is reversed [33]. This problem is addressed in the dual-tunnel valve. In Section 2 of this article, we saw that by placing symmetric reference layers above and below the free layer, it is possible to nearly cancel the spin-transfer torque on the free layer.

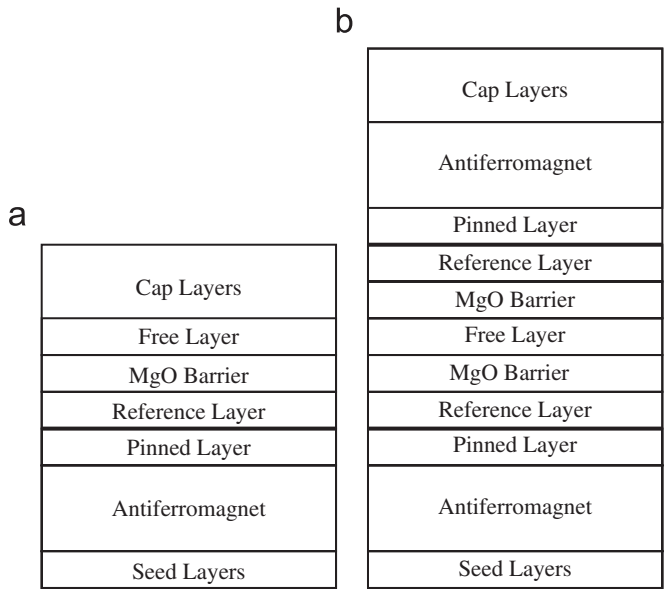

Fig. 5. Schematic representation of a simple (a) and dual (b) MRAM stack. Unlike Fig. 3, the pinned layer magnetizations in the dual stack are oriented anti-parallel to one another.

As shown in Fig. 5b, in the dual-tunnel valve, reference layers are placed above and below the free layer, and the reference layer magnetizations are anti-parallel to one another. This can be achieved in several ways–for example, using antiferromagnets with different blocking temperatures so each layer can be set independently. For read back it is important that the barriers have substantially different MR ratios, or it would be difficult to detect a resistance change associated with free layer reversal. Despite the necessary asymmetry between the two free/reference layer interfaces, a dual stack design will reduce the polarity asymmetry of the write currents. In the first implementations of this concept, the top spacer layer was Cu [34,35]. Recently, Diao et al. [36] have successfully built devices with dual MgO barriers, which exhibited a threefold reduction in average I_c compared to simple MgO stacks. In addition to superior symmetry, dual tunnel barriers are desirable because they avoid the "spin pumping" at the free layer/Cu interface which may increase the effective damping [37]. There may be additional materials or architectures to improve the writing properties. For example structures that include reference layers with both in-plane and out-of-plane anisotropy layers may increase the write efficiency or decrease the write times [38–40].

For simplicity, we have been assuming that the free layer and reference layer are collinear. For reliable operation, it will likely be necessary to cant the reference layer at some known angle. As Krivorotov et al. [41] have shown, this minimizes the effect thermal fluctuations will have on the initial torque and produces more reproducible switching. It may also prove useful to judiciously position the leads to the MTJ so that the Oersted field from the current pulse can assist in the reversal process, though the impact of this Oersted field will grow less important as device dimensions are reduced. Finally, it may be helpful to include a small hard bias field ($\sim\frac{1}{3}$ H_k) orthogonal to the easy axis to accelerate the switching process [36,42].

Before 2004, spin-transfer reversal in an MTJ had yet to be observed. Over the past 3 years remarkable progress has occurred. At the end of 2005, Sony announced a 4 kB ST-MRAM demonstration [43], and in February 2007, a Hitachi/Tohuku collaboration announced a 2 Mbit ST-MRAM demo [44]. The Hitachi demo used a simple rather than dual MgO MTJ stack, so, despite the rather large current densities ($\sim 6\times10^6$ A/cm^2) used, the switching was operated in the thermally assisted regime (100 ns write time). The recent Grandis dual MgO work demonstrates fairly symmetric switching that extrapolates to J_c values around 1×10^6 A/cm^2. Over the next several years, it is not inconceivable to imagine current densities dropping an additional factor of two, and approaching the 5×10^5 A/cm^2 required for a single minimum dimension transistor to program the bit. At that point, it will be interesting to see if any company is willing to devote the resources that would be necessary to move ST-MRAM past the demonstration phase, and attempt to commercialize the technology. Although there are significant engineering challenges that would confront such a commercialization attempt, we see no fundamental obstacles that would prevent ST-MRAM from becoming a "nearly universal" memory. At low storage densities, one is free to use a large transistor to provide current pulses strong enough to produce switching performance comparable to SRAM, while slower performance should allow the bit density to approach that of single level flash. Though it will require significant materials advances, it is even possible that ST-MRAM will eventually provide fast performance at high density.

4. Current-tunable oscillators

For MRAM applications, the spin-transfer effect is used to reverse the magnetization of a bit. In the presence of a large magnetic field, the spin-transfer torque can drive uniform precession of the free layer magnetization about the axis of this applied field. This high-frequency precession has been studied in metallic multilayers in both nanopillar [45] and point contact [46] geometries. When coupled with the GMR effect, this precession produces a voltage response that makes these devices high-frequency oscillators.

These nanoscale spin-transfer oscillators can have frequencies ranging perhaps as high as 100 GHz, have demonstrated linewidths as narrow as 2 MHz, and the frequency can be tuned by adjusting the current. Hence, the spin-transfer effect provides a means of producing an agile, nanoscale, GHz radiation source that can be fabricated on a chip. Potential applications for such a source include phased-array transceivers, and chip-to-chip, as well as wireless on-chip communication [25].

One barrier that stands in the way to practical use of such oscillators is eliminating the need for an external field

that is used in most experimental demonstrations. As discussed in Section 2, hard magnets are integrated into today's recording heads to provide bias fields for the sensor. The bias materials from today's disk drives could easily provide 3 kOe of field for spin-transfer oscillators, and perhaps significantly larger fields could be obtained from other materials. Alternatively, a large effective field could be applied to the free layer by indirect exchange coupling to a fixed magnetic layer as discussed in Ref. [47]. One could eliminate the need for external fields in an oscillator if free layers with very large anisotropy fields were used or by combining layers with in-plane and out-of-plane anisotropy. Theoretical predictions of in-plane and out-of-plane structure that could form tunable oscillators [39] have recently been experimentally realized [48].

Increased output power is a more difficult technical challenge that these oscillators must overcome before they will be useful for applications. The best metallic spin-transfer oscillators measured to date produce about 100 pW, while a few microwatts would likely be required for practical GHz communication applications. Are such power levels attainable? In a fully metallic system, it may be possible. The first step would be to increase the power output from an individual oscillator. If high polarization materials like Heusler alloys are used, it would increase the GMR signal and hence the power output from the oscillator, but even if a single device were to achieve 1 nW, approximately three orders of magnitude more power output is required. Phase locking may offer a path to these power levels. Groups at Freescale [49] and NIST/HGST [50] have recently demonstrated phase locking in closely spaced point contact oscillators. In a follow-on experiment, the NIST group demonstrated that spin waves propagating through the continuous free layers were responsible for the phase locking [51], though other means of phase locking may be available as well [52]. If phase locking is achieved for a collection of N oscillators, depending on how the devices are wired, the maximum output power may grow as quickly as N^2 [52]. In this best case scenario, to achieve $1000\times$ more power, over 30 oscillators would be required. As no more than two coupled oscillators have been demonstrated to date, considerable further work is required before the feasibility of large-scale arrays and the maximum power achievable from such an array can be evaluated.

Such arrays may not be required if tunnel valve oscillators can be used. To our knowledge, there are no published reports of high-frequency spin-transfer oscillations in MTJs, but the MgO films appropriate for observing these effects have only recently become available. These films can only withstand around 10^7 A/cm^2, which is typically less than the current densities at which these oscillations have been observed in metallic systems. As discussed in the MRAM section of this paper, MgO films appear to have very high spin-transfer efficiencies. In addition, the thermal stability requirement on the free layer that exists for MRAM is no longer relevant for spin-transfer oscillators so low-moment free layers with correspondingly lower critical currents are viable options.

Assuming that it will be possible to build a nano spin-transfer oscillators with a MgO tunnel valve, what output power might be expected from such a device? As a conservative estimate, assume a single oscillator operating at $J = 10^6$ A/cm^2, with RA $= 5\,\Omega\mu$m^2, and $\Delta R/R = 100\%$. Further assume we excite a uniform precession in which 10% of the TMR output is utilized. Roughly speaking, such a device would produce P (in Watts) $= 10^4 \times$ Area (in cm^2), or 0.5 μW for a single 50×100 nm device. From this estimate, it appears that MTJ oscillators may offer a means to achieving useful output powers without requiring large, phase-locked arrays.

In concluding this section, we wish to emphasize that compared to ST-MRAM, spin-transfer oscillators are in a relative state of infancy, so a great deal of fundamental work remains to be done before their true feasibility for GHz applications can be evaluated.

5. Summary

What does the future hold for spin-torque device applications? For the foreseeable future, spin-torque effects will play an important role in the design and performance of CPP sensors. For high-frequency oscillator applications, research is still in the very early stages, but reaching sufficient output powers appears to be the main technological hurdle that needs to be overcome. Considerably more research has been done investigating the feasibility of ST-MRAM. Although we see no fundamental barriers to building such a memory, there are many competing technologies vying to enter this market. Whether or not we see commercial ST-MRAM in widespread applications or only entering niche markets may depend not only on how quickly ST-MRAM can solve the challenges outlined in this paper, but also on the rate that competing memory technologies, especially those that are silicon-based, continue to advance. In addition to applications discussed here, new opportunities such as current driven domain-wall motion for memory and logic applications [53–55] are likely to emerge as new physical phenomena are uncovered in the area of spin torque.

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